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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,010	07/22/2003	Kevin Weaver	100-22400 (PO5620)	8431

33402 7590 11/29/2005

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,010	WEAVER ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23,25,28 and 35-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *38-50* is/are allowed.

6)☒ Claim(s) *23,25,28,35-37 and 51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/14/2005 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

2. **Claims 23, 25, 28, 35-37, and 51** are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "test" in claims 23, 25, 28, and 35-37 is used by the claim to mean "repair" or "edit", while the accepted meaning is "**1.** A procedure for critical evaluation; a means of determining the

presence, quality, or truth of something; a trial: *a test of one's eyesight; subjecting a hypothesis to a test; a test of an athlete's endurance.* **2.** A series of questions, problems, or physical responses designed to determine knowledge, intelligence, or ability. **3.** A basis for evaluation or judgment: *"A test of democratic government is how Congress and the president work together"* (Haynes Johnson). **4.** *Chemistry* **a.** A physical or chemical change by which a substance may be detected or its properties ascertained. **b.** A reagent used to cause or promote such a change. **c.** A positive result obtained. **5.** A cupel." (The American Heritage® Dictionary of the English Language, Fourth Edition.).

The term is indefinite because the specification does not clearly redefine the term. In the mentioned claims, the elements of the claimed test structure are clearly for editing purposes (the claims and specification, page 1 to page 9, including the title). The specification mentions: "Thus, the present invention allows design fixes to be implemented and tested without incurring the delay in time and the significant expense that are required to first obtain new photolithographic mask set revisions, and then fabricate new parts that include the added resistance", but this is not the same as "clearly redefine the term". The invention and the claimed invention are about implementing an electrical element, i.e., a resistive element or a capacitive element, to an almost-finished die or a bare die. The finished product is then invariably tested for functionality, but the recited test structure does not take part in the testing procedure, the claimed test structure only includes the implemented elements.

Claim 51 depends from rejected claim 23 and includes all limitations of claim 23, thereby rendering the claim indefinite.

For examination purposes, at this stage of the prosecution, the "test structure" is treated as an "electrical structure".

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 23 and 51** are rejected under 35 U.S.C. 102(b) as being anticipated by Worley et al. U.S. Patent 6,147,857 (the '857 reference).

The '857 reference discloses in the figures, particularly Fig. 1, and respective portions of the specification a semiconductor device as claimed.

IC1. Referring to **claim 23**, the reference discloses a semiconductor device comprising:

a die (generally indicated at the structure comprising silicon substrate 123 and structure 122, Fig. 1) having:

a semiconductor structure (123) that includes a substrate (123) and a plurality of devices (one of which is a transistor comprising source/drain regions 124/110 and gate 113) that are formed in and on the substrate (This reference is introduced also to prove that in the pertinent art, a die having an integrated active circuit comprises a semiconductor structure that includes a substrate and a plurality of devices that are formed in and on the substrate); and

an interconnect structure (generally indicated at 122) connected to the semiconductor structure to electrically interconnect the devices to realize a circuit, the interconnect structure having a top surface, a dielectric structure (generally indicated at 122), a first metal region (114a, see below or next page) that contacts the dielectric structure, and a second metal region that contact the dielectric structure; and

an electrical structure including:

a first conductive region (102, column 3, last full paragraph) having a first surface connected to an exterior surface of the interconnect structure and an opposing second surface;

an insulation region (101) having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region; and

a second conductive region (a region of layer or region 100) having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region.

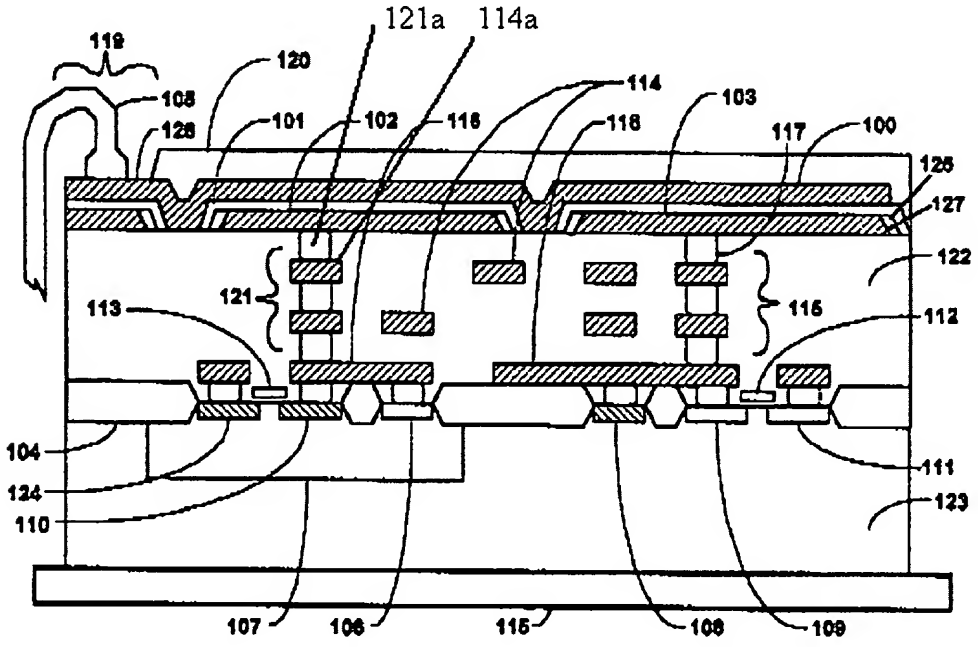

Fig. 1

121a and 114a are added for ease of explanation

Referring to **claim 51**, the reference further discloses a first opening (generally indicated at 121a) formed in the dielectric structure, the first opening extending from the top surface down to the first metal region; and

a first conductive structure (121a) formed in the first opening, the first conductive structure being electrically connected to the first metal region (114a) and the first conductive region (102).

4. **Claims 23, 25, and 51** are rejected under 35 U.S.C. 102(b) as being anticipated by Leung et al. U.S. Patent 5,789,303 (the '303 reference).

The '303 reference discloses in the figures, particularly Fig. 3, and respective portions of the specification a semiconductor device as claimed.

IC2. Referring to **claim 23**, the reference discloses a semiconductor device comprising:

a die (generally indicated at the structure below and including passivation layer 116, Fig. 3, paragraph bridging columns 7 and 8, wherein the die comprises a semiconductor substrate 102 which itself includes not-shown active devices together with not-shown metal levels and not-shown interlevel dielectric (ILD) layers , a top metal layer 104/106, a top ILD 114, and a passivation layer 116. This reference is introduced also to prove that in the pertinent art, a die of a device including a die (chip) and an on-chip capacitor, most everything below the on-chip capacitor is the chip (die)) having:

a semiconductor structure that includes a substrate (generally indicated at 102, Fig. 3) and a plurality of devices (not shown) that are formed in and on the substrate (see paragraph IC1 above); and

an interconnect structure (generally indicated at 106/104/114/116 and part of 102) connected to the semiconductor structure to electrically interconnect the devices to realize a

circuit, the interconnect structure having a top surface, a dielectric structure (114), a first metal region (104) that contacts the dielectric structure, and a second metal region (106) that contact the dielectric structure; and

an electrical structure including:

a first conductive region (128, column 8, lines 15-36) having a first surface connected to an exterior surface of the interconnect structure and an opposing second surface;

an insulation region (130) having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region; and

a second conductive region (134) having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region.

Referring to **claim 25**, the reference further discloses a first opening (generally indicated at 124) formed in the dielectric structure (114), the first opening extending from the top surface down to the first metal region (104);

a first conductive structure (124) formed in the first opening to electrically connect the first metal region (104) and the first conductive region (128) of the electrical structure;

a second opening (generally indicated at 124) formed in the dielectric structure (114), the first opening extending from the top surface down to the second metal region (106);

a second conductive structure (124) formed in the second opening to electrically connect the second metal region (106) and the second conductive region (134) of the electrical structure.

Referring to **claim 51**, the reference further discloses a first opening (generally indicated at 124) formed in the dielectric structure (114), the first opening extending from the top surface down to the first metal region (104); and

a first conductive structure (124) formed in the first opening, the first conductive structure being electrically connected to the first metal region (104) and the first conductive region (128).

5. **Claims 23, 25, and 51** are rejected under 35 U.S.C. 102(e) as being anticipated by List et al. U.S. Patent Application Publication 20030001284 (the '284 reference).

The '284 reference discloses in the figures, particularly Fig. 1, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 23**, the reference discloses a semiconductor device comprising:

a die (not shown, paragraphs [0004] for ICs with transistors, [0002] for an overall structure, and [0024] for the not-shown feature, and see paragraph IC1 and IC2 above) having:

a semiconductor structure that includes a substrate (not shown) and a plurality of devices (not shown) that are formed in and on the substrate (see paragraph IC1 above); and

an interconnect structure (generally indicated at 10/72/74/76, Fig. 1) connected to the semiconductor structure to electrically interconnect the devices to realize a circuit, the interconnect structure having a top surface, a dielectric structure (generally indicated at 10 or not shown), a first metal region (72 or not shown) that contacts the dielectric structure, and a second metal region (74 or not shown) that contact the dielectric structure; and

an electrical structure (generally indicated at the structure of Fig. 1 not including the interconnect structure) including:

a first conductive region (18, paragraph [0025]) having a first surface connected to an exterior surface of the interconnect structure and an opposing second surface;

an insulation region (16) having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region; and

a second conductive region (14 or generally indicated at 14/84) having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region.

Referring to **claim 25**, the reference further discloses a first opening (generally indicated at 72) formed in the dielectric structure (10), the first opening extending from the top surface down to the first metal region (not shown);

a first conductive structure (72) formed in the first opening to electrically connect the first metal region (not shown) and the first conductive region (18) of the electrical structure;

a second opening (generally indicated at 74) formed in the dielectric structure (10), the first opening extending from the top surface down to the second metal region (not shown);

a second conductive structure (74) formed in the second opening to electrically connect the second metal region (not shown) and the second conductive region (14 or 14/84) of the electrical structure.

Referring to **claim 51**, the reference further discloses a first opening (generally indicated at 72) formed in the dielectric structure (10), the first opening extending from the top surface down to the first metal region (not shown); and

a first conductive structure (72) formed in the first opening, the first conductive structure being electrically connected to the first metal region (not shown) and the first conductive region (18).

Allowable Subject Matter

6. Claims 28 and 35-37, insofar as in compliance with the 112 rejection detailed above, and claims 38-50 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance: The prior art of record fails to teach or render obvious a semiconductor device with all exclusive limitations as recited in claims 28 and 38, including the respective die having the respective interconnect structure including a dielectric structure and a top surface, characterized in that a third opening is formed in the dielectric structure and extends from the top surface down through the metal trace to break an electrical connection between the first and second regions of the metal trace (claim 28) or that a region of silicon having a bottom surface is connected to only a non-conductive region of the top surface of the interconnect structure and is spaced apart from the bond pads.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
November 19, 2005